Claims

1. A cooling stage for a semiconductor substrate comprising:

a pedestal having a substantially planar top surface,

a first plurality of grooves concentrically formed in said top surface, and

a second plurality of linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with said first plurality of circular grooves allowing a cooling fluid to flow therethrough when said semiconductor substrate is positioned on said top surface of the pedestal.

2. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality is at least 3 and said second plurality is at least 2.

3. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality is preferably at least 5 and said second plurality is preferably at least 3.

4. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality of circular grooves and said second plurality of linear grooves each having a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm.

5. A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality of circular grooves and said second plurality of linear grooves each having a width

preferably between about 3 mm and about 5 mm, and a depth preferably between about 1 mm and about 3 mm.

6. A cooling stage for a semiconductor substrate according to claim 1, wherein said cooling stage being situated in a cool-down chamber in a cluster tool for sputtering of metals on semiconductor wafers.

7. A cooling stage for a semiconductor substrate according to claim 1, wherein said cooling stage being used in a cool-down chamber positioned between a high temperature sputtering process and a low temperature sputtering process for cooling down a wafer.

8. A method for cooling a semiconductor substrate comprising the steps of:

providing a cooling stage comprising a wafer pedestal equipped with a grooved top surface thereon, said grooved top surface comprises a first plurality of circular grooves concentrically formed in said top surface and a second plurality of linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with said first plurality of circular grooves,

positioning a heated semiconductor substrate on said grooved top surface,

flowing a cooling liquid through a cooling channel in said wafer pedestal to carry away hat transferred to said grooved top surface, and

flowing a cooling gas through said first and second plurality of circular and linear grooves to carry away heat from a backside of said heated semiconductor substrate.

9. A method for cooling a semiconductor substrate according to claim 8, wherein said grooved top surface further comprises at least 3 circular grooves and at least 2 linear grooves.

10. A method for cooling a semiconductor substrate according to claim 8, wherein said grooved top surface comprises preferably at least 5 circular grooves and at least 3 linear grooves.

11. A method for cooling a semiconductor substrate according to claim 8 further comprising the step of providing said grooved top surface with a plurality of circular and linear grooves, each having a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm.

12. A method for cooling a semiconductor substrate according to claim 8 further comprising the step of providing said grooved top surface with a plurality of circular and linear grooves, each preferably having a width between about 3 mm and about 5 mm, and a depth of between about 1 mm and about 3 mm.

13. A method for cooling a semiconductor substrate according to claim 8 further

comprising the step of positioning a semiconductor substrate exiting a high temperature sputtering chamber on said grooved top surface of said cooling stage.

14. A method for cooling a semiconductor substrate according to claim 8 further comprising the step of removing a cooled-down semiconductor substrate from said cooling stage and positioning the substrate in a low temperature sputter chamber.

15. A method for cooling a semiconductor substrate according to claim 8 further comprising the steps of flowing a cooling liquid through said cooling channel in said wafer pedestal, and flowing a cooling gas of an inert gas through said first and second plurality of circular and linear grooves.

16. A wafer pedestal effective in cooling a high temperature processed wafer comprising:

a wafer pedestal having a substantially planar top surface,

at least 3 circular grooves concentrically formed in said top surface, and

at least 2 linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with said at least 3 circular grooves such that a cooling fluid flows through said circular and said linear grooves to cool said high temperature processed wafer positioned thereon.

17. A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16, wherein said wafer pedestal being positioned in a cool-down chamber positioned between a high temperature sputter chamber and a low temperature sputter chamber.

18. A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16, wherein said wafer pedestal preferably comprises at least 5 circular grooves and at least 3 linear grooves.

19. A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16 further comprising 9 circular grooves and 3 linear grooves each having a width of about 2 mm and a depth of about 1 mm.

20. A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16, wherein said cooling fluid flown through said circular and said linear grooves is an inert gas selected from the group consisting of argon, nitrogen and helium.